REMARKS

Claims 1-7, 9 and 10 are pending in the present application, claim 8 having been cancelled without prejudice to re-file in a divisional application and claims 9 and 10 having been added herein. The Office Action and cited references have been considered. Favorable reconsideration is respectfully requested.

In the Office Action, the Examiner sets forth in writing the election requirement previously made by telephone. The Examiner has restricted the claims to two inventions, group I including claims 1-7 and group II including claim 8. Applicant confirms the provisional election previously made to prosecute the invention of group I, claims 1-7.

The drawings were objected to because the drawing elements were not labeled in English. Substitute drawings are attached herewith which provide the labels in English. Withdrawal of this objection is respectfully requested.

The drawings were also objected to because the reference character "25" had allegedly been used to designate both I2C buses and 8-bit decoder components as claimed in claim 5. It is noted that the bus 10 is an "I2C" bus developed by Phillips (see page 5, lines 17-18 of the description), and not "12C" as mentioned in the Office Action. Applicant has amended claim 5 to clarify that the three eight-bit decoder components 25 are actually bus decoders for bus I2C (see for example page 7, lines 16-20 of the description). Accordingly, claim 5 now recites three eight-bit I2C bus decoder components 25. Withdrawal of this objection is respectfully requested.

Claims 1 and 5 were objected to based on a number of informalities. These informalities have been corrected. Withdrawal of the objection is respectfully requested.

Claims 5 and 7 were rejected under 35 U.S.C. § 112, second paragraph. With respect to claim 7, the term "ASCII format" is deleted from the claim, rendering this objection moot. With respect to claim 5, the rejection is traversed. As described on page 7, lines 17-20 of the description, the bus decoder component 26 serves for transferring data retrieved from the memory components 22 to the I2C bus, while the other three bus decoder components 25 serve for addressing the memory components 22, on the basis of the information coming from the I2C bus (see figs. 2 and 4). In addition, there is only one I2C internal communication bus 10 and no selection among several I2C buses is required.Thus, Applicant respectfully submits that the amendment of claim 5 proposed by the Examiner is not appropriate. Applicant respectfully submits that the claimed structure and function would be understood by one of ordinary skill in the art reading the application and reviewing the drawings as originally filed. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-7 were rejected under 35 U.S.C. § 103 as being unpatentable over Huffman et al. (WO 97/23819), in view of well known features of which official notice was taken. This rejection is respectfully traversed.

Claim 1 recites a device for the storage and searching of textual and graphical information in electronic form, the device comprising a case (1), a display means (9), a user interface means (3), an operating means (11), a means for

storage (5) of the information, a means of selecting information to be displayed according to the user's instructions, and a multiplexed address bus (10). This is not taught, disclosed or made obvious by the prior art of record.

Huffman uses a well-known technology, which is a PCMCIA card (see page 5, line 27 and figure 37). This card operates with a parallel bus which has those very same drawbacks that are mentioned in the opening portion of the description of the present invention (see from page 4, line 11 to page 5, line 3): a high volume because of the high number of connections, and high power consumption, in addition to prohibitive manufacturing complexity and production costs.

Because of the use of a multiplexed address bus, the invention as claimed makes it possible to reduce in a very significant manner the number of connections: the I2C bus is a two-wire bus with two power supply wires, i.e. four wires in total, instead of 64 in Huffman.

Not only does the use of such a bus improve performance reliability, in comparison with a PCMCIA card, since the reduced number of connections reduces the risk of card malfunction, but it also provides ease of use, it saves space, and it lowers overall cost.

Moreover, the internal architecture of the PCMCIA card is convenient for low-speed systems with limited storage capacity, but it is not suitable at all for rapid access to a very large volume of information as is required within the context of the present invention.

Therefore, in brief, a person skilled in the art would not turn to Huffman for solving the technical problem of

providing large storage capacity and rapid access to a large amount of stored information in a compact and inexpensive device, because the memory card disclosed by Huffman has all the drawbacks that it is desired to overcome. The Applicant respectfully submits that the teaching of Huffman would not lead a person skilled in the art to the invention as claimed.

Further, whether or not a multiplex address bus is known in the prior art is asserted in the Office Action, is not in and of itself sufficient to render the claims obvious in view of Huffman. In particular, there must be a teaching or motivation taught in the prior art to modify the patented device as suggested in the Office Action. Applicant respectfully submits that only with impermissible hindsight reference to Applicant's disclosure would such a modification have been obvious to one of ordinary skill in the art. Huffman says nothing about the advisability of reducing the number of connections or the advantages attendant therewith. The Taylor Patent (U.S. Patent No. 5,835,965) cited in the Office Action as allegedly teaching the advantages of using multiplexed address buses to reduce the number of pins to be used in addressing memory devices does not satisfy this deficiency. In col. 2, lines 43-49, Taylor specifically teaches against using multiplexed address ports because, as he says, the system is more complicated and increases device and system cost. Accordingly, in the absence of Applicant's disclosure, one of ordinary skill in the art would not have been motivated to modify the device of Huffman to include a multiplexed address port.

For at least these reasons, Applicant respectfully submits that claim 1 is patentable over the prior art of record whether taken alone or in combination as proposed in

the Office Action. Claims 2-7 are believed to be patentable in and of themselves and as they depend from and include the recitations of claim 1, which is patentable for the reasons discussed above.

Moreover, with respect to claim 5, the Examiner has not set forth a *prima facie* case of obviousness. The Examiner has not cited a piece of prior art or any combination of prior art that teaches the construction of the storage means as claimed in claim 5. Only with impermissible hindsight reference to Applicant's disclosure would one of ordinary skill in the art have come up with Applicant's claimed invention.

In view of the above amendments and remarks, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections of record. Applicant submits that the application is in condition for allowance and early notice to this effect is most earnestly solicited.

If the Examiner has any questions he is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

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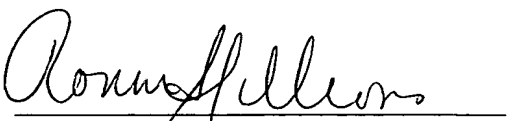
Attorneys for Applicant

By 
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Amendments to the Drawings

Attached to this paper are replacement drawings for Figs. 3-7 as well as annotated sheets showing changes to the original drawings.

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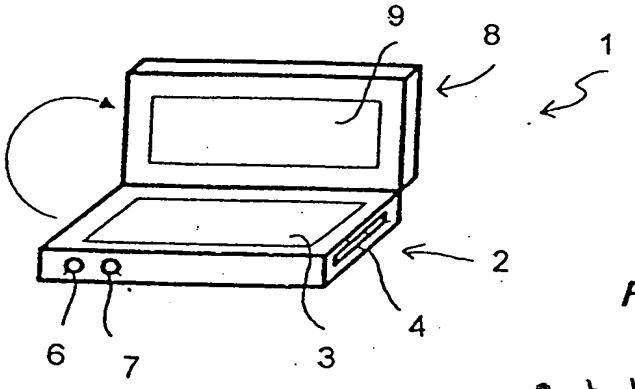

Fig. 1

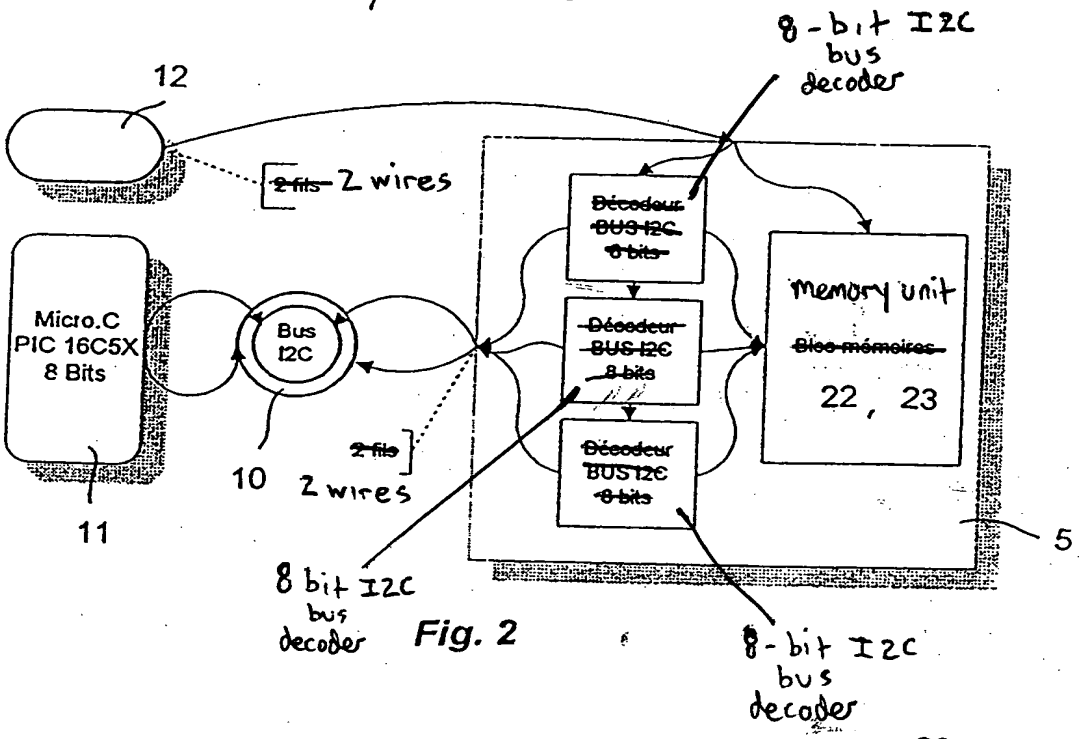

Fig. 2

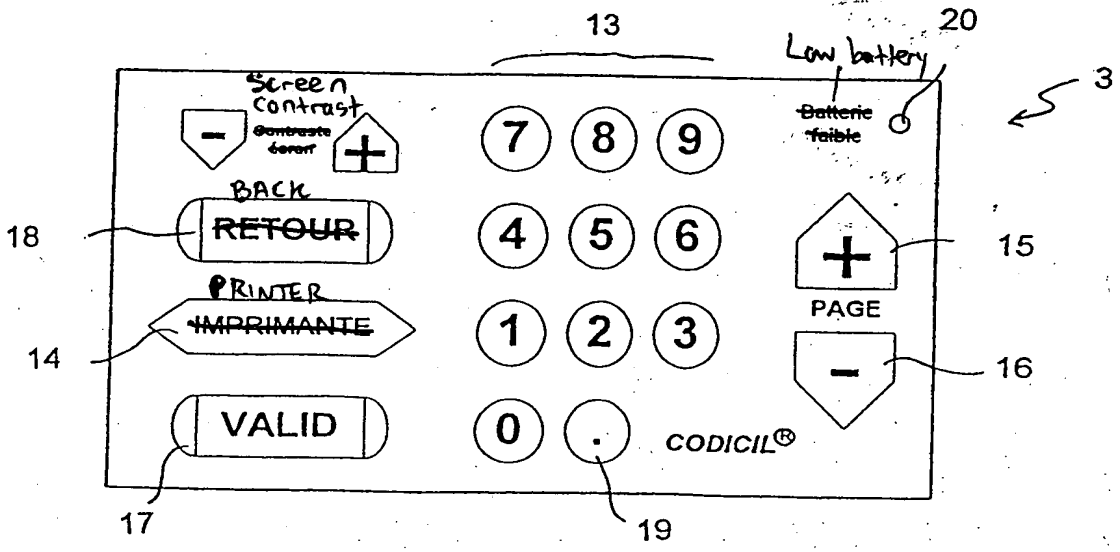

Fig. 3

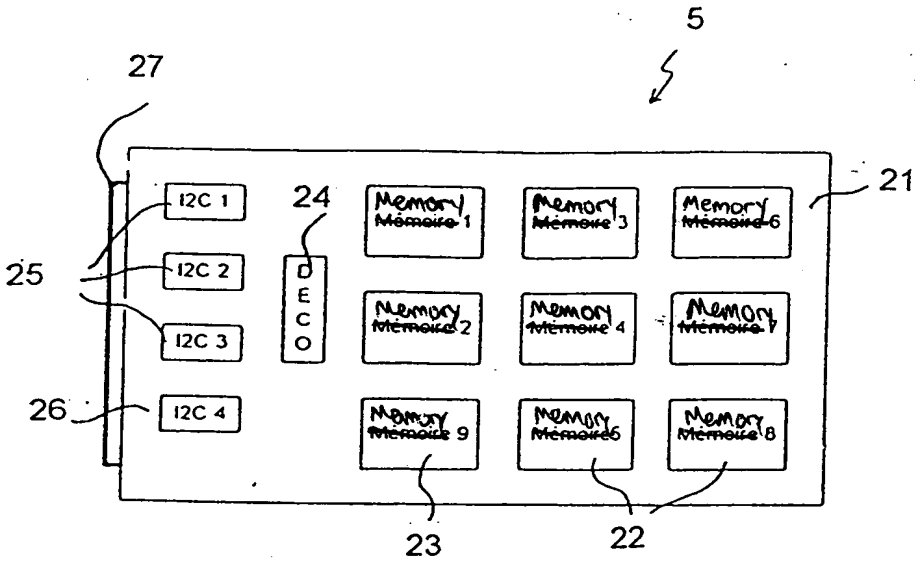

Fig. 4

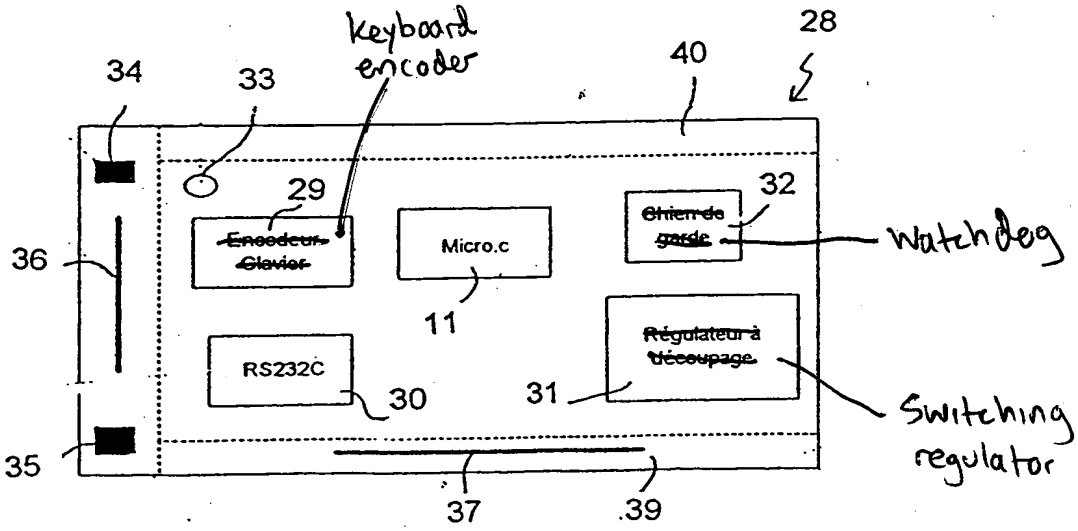

Fig. 5

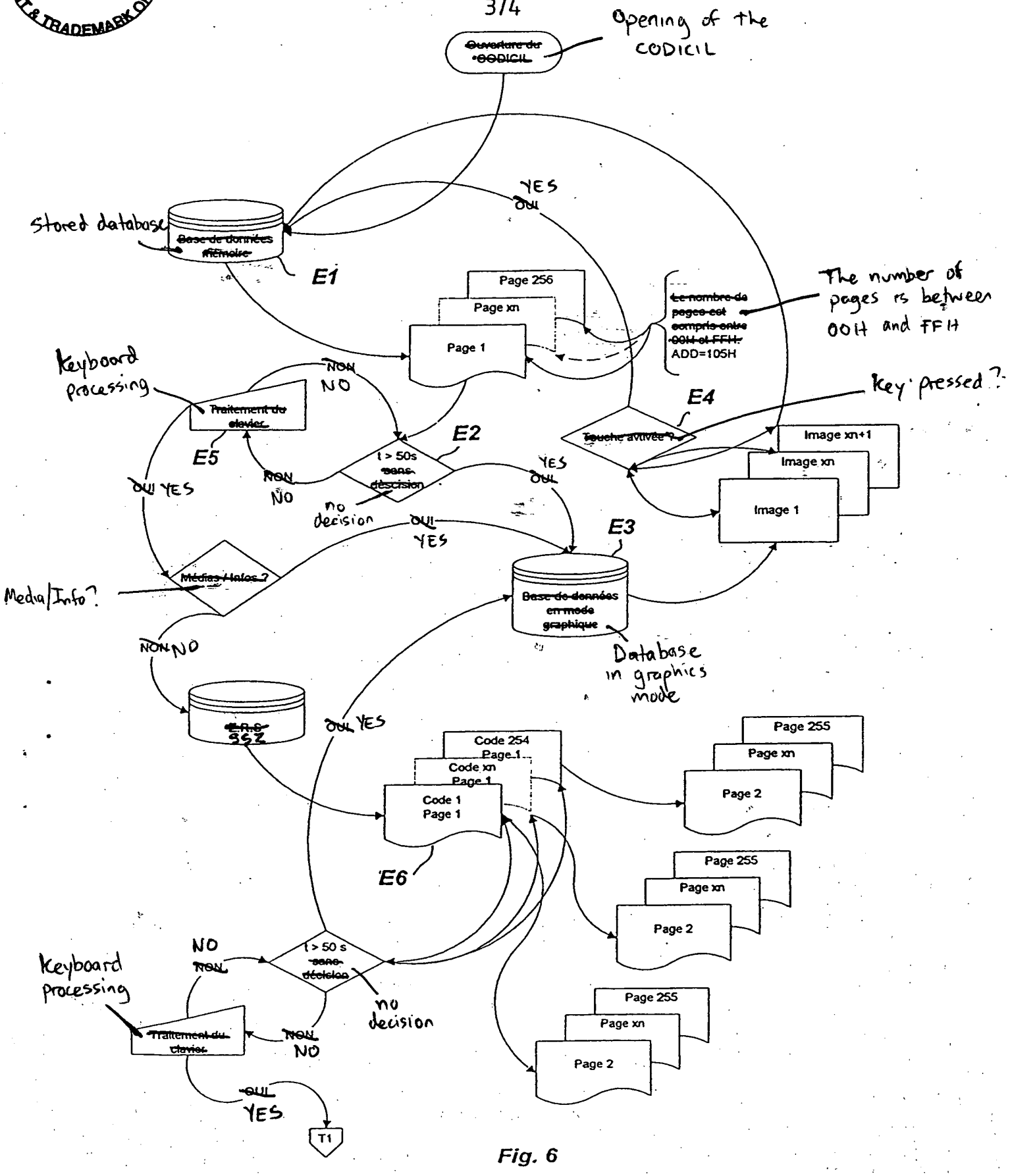

Fig. 6

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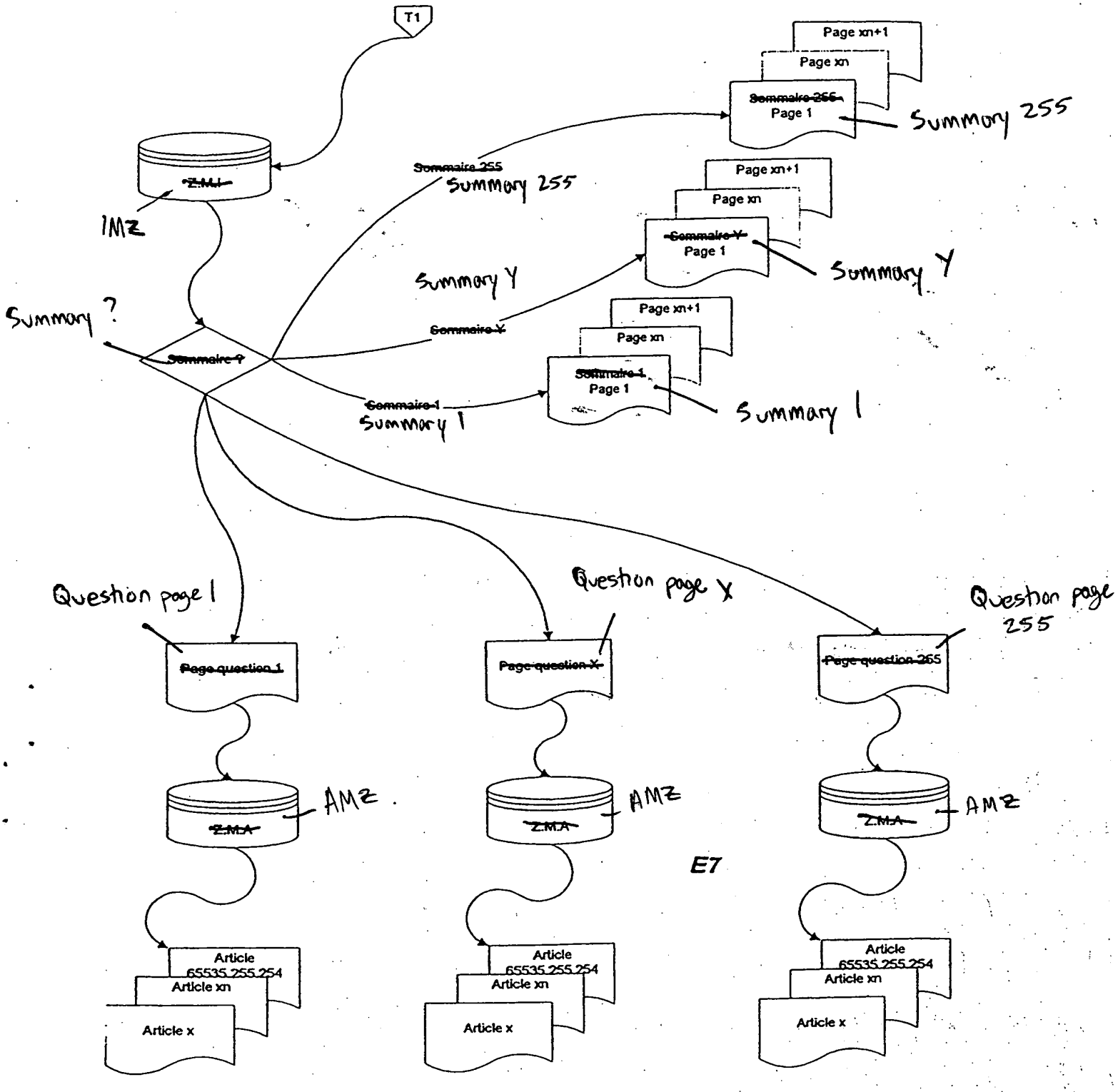

Fig. 7